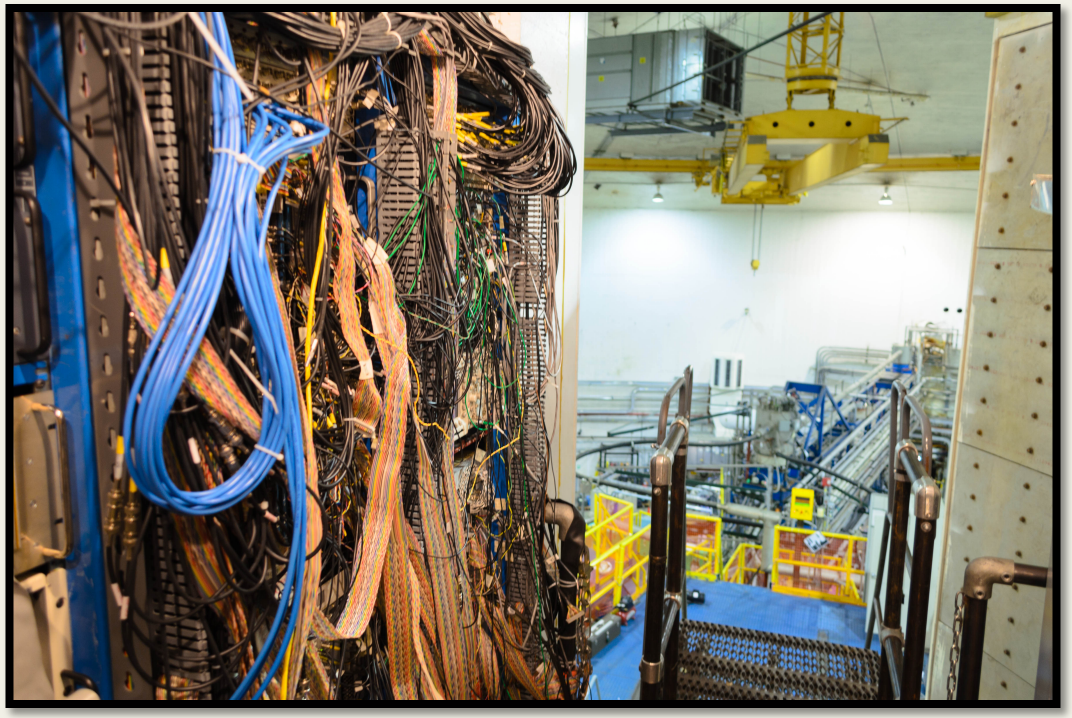
Hall A DAQ Status

And Performance Update



Ryan Zielinski

UNIVERSITY of NEW HAMPSHIRE

Hall A Collaboration Meeting – June 7, 2012

Outline

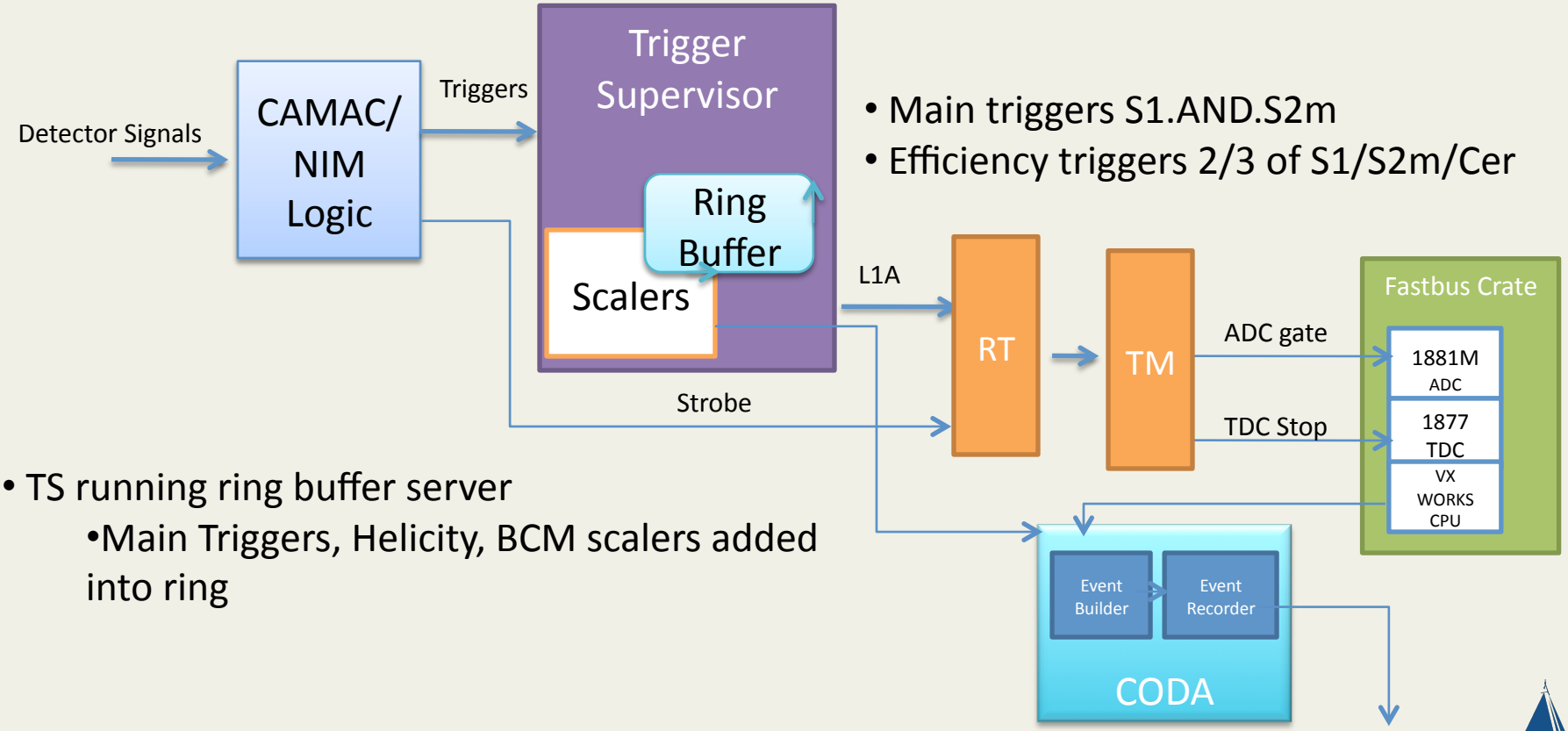
- g2p/gep DAQ Setup
  - Single Arm HRS DAQ
  - HAPPEX DAQ

- Improving Performance – Lower Deadtime
  - Additional HRS FASTBUS crate
  - SFI Sequencer
  - Intel/Linux CPU

- g2p/gep DAQ performance

HRS DAQ

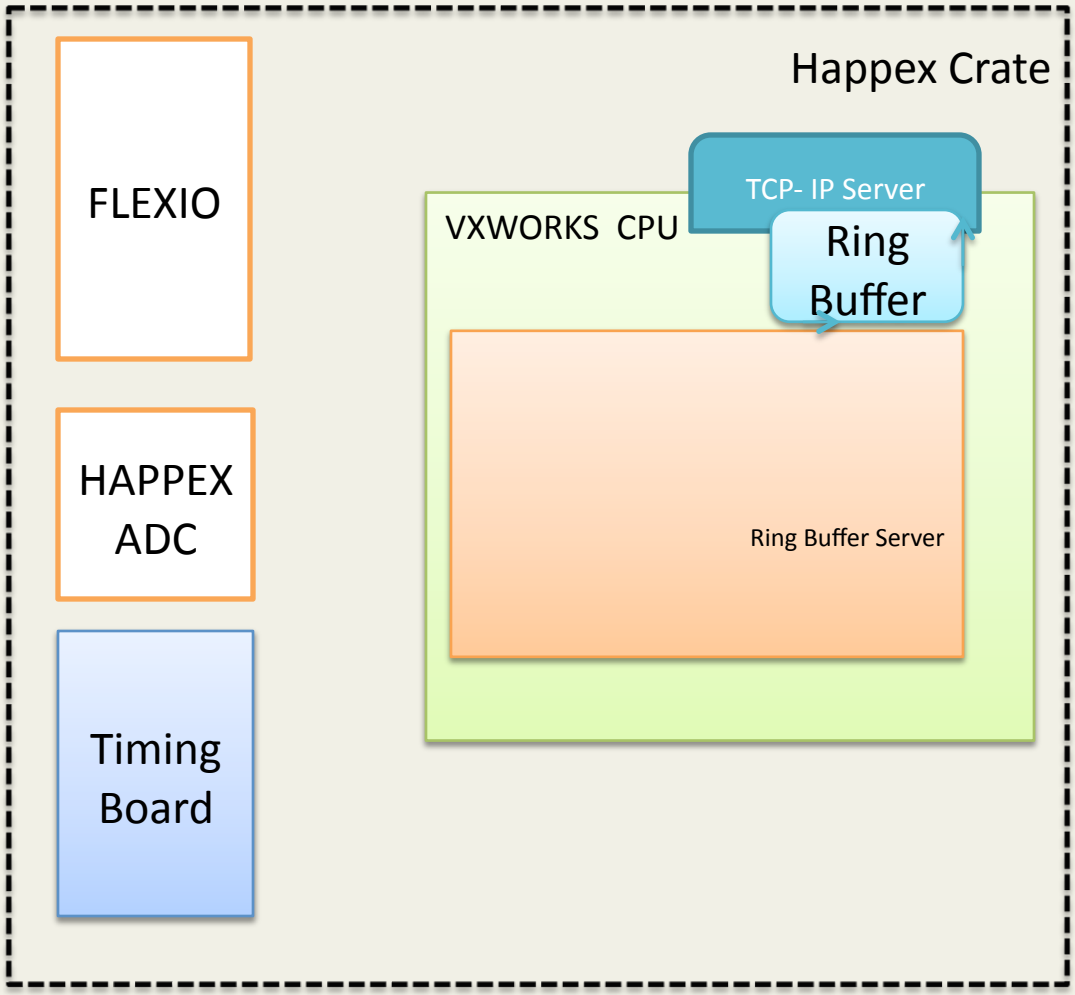
- LHRS and RHRS DAQ operate independently (singles)
- 3 fastbus crates, TS scaler crate and HAPPEX crate on each arm



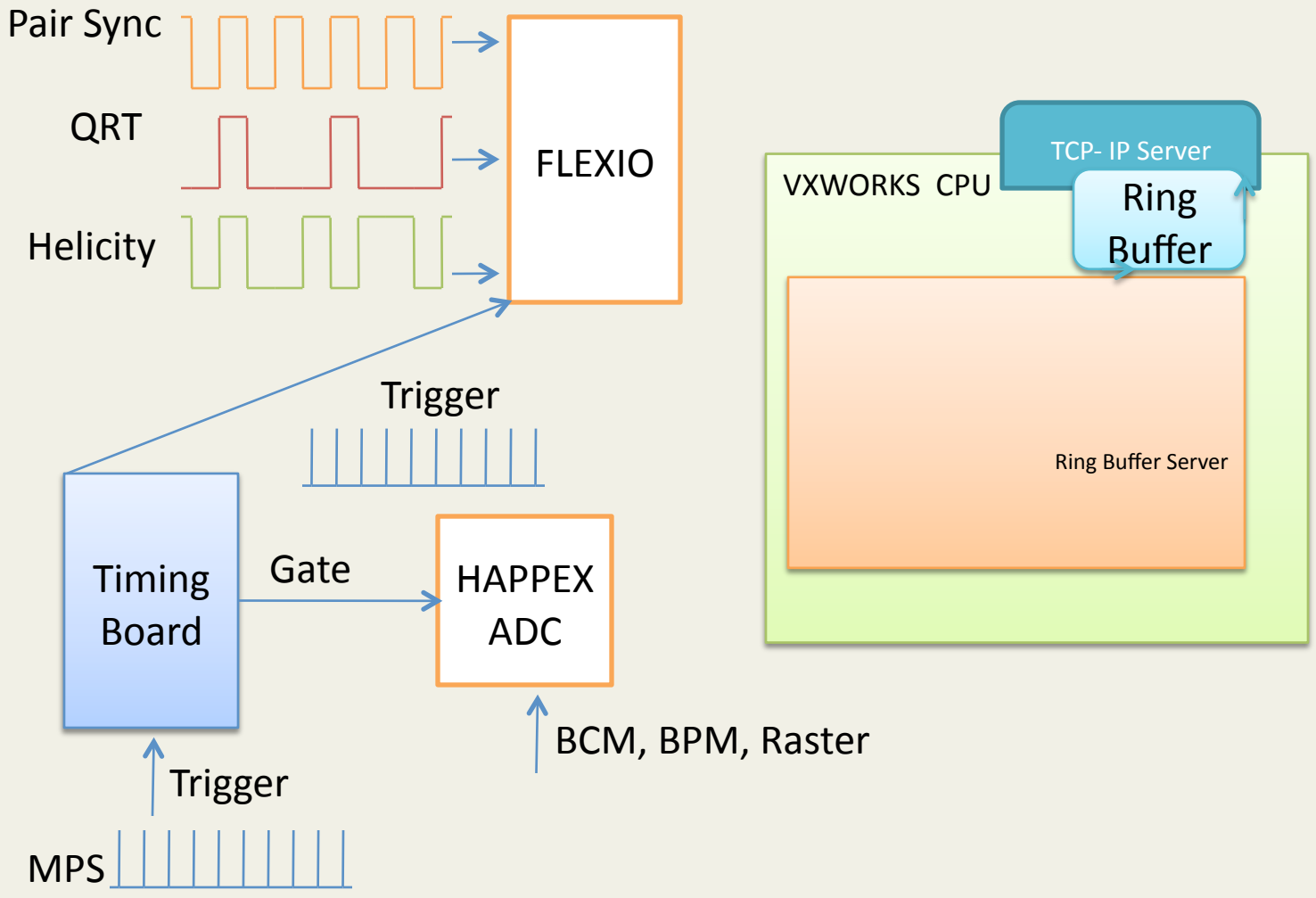
- Main triggers S1.AND.S2m
- Efficiency triggers 2/3 of S1/S2m/Cer

- TS running ring buffer server
  - Main Triggers, Helicity, BCM scalers added into ring

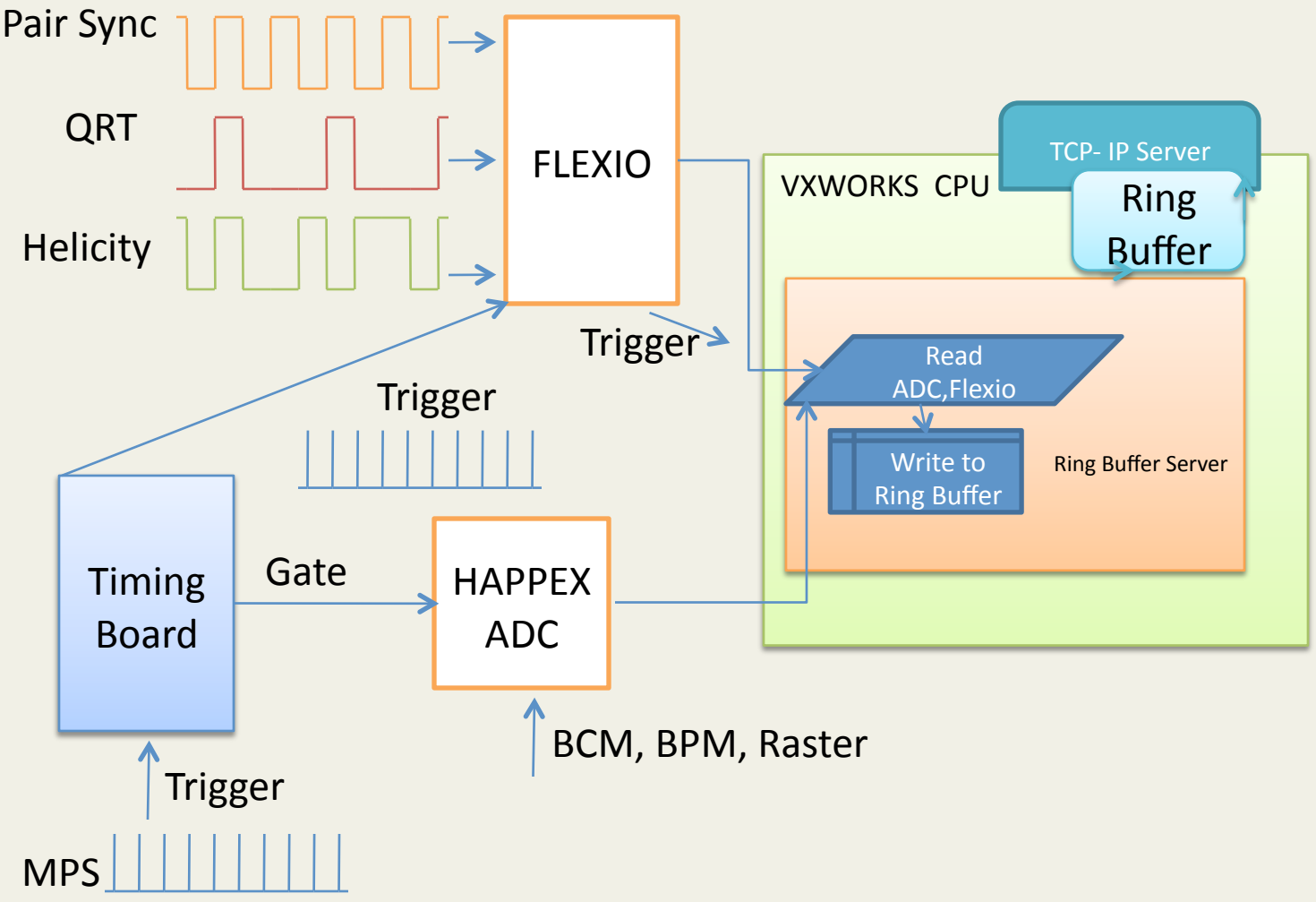
HAPPEX DAQ


Happex Crate
FLEXIO
HAPPEX ADC
Timing Board
VXWORKS CPU
TCP- IP Server
Ring Buffer
Ring Buffer Server

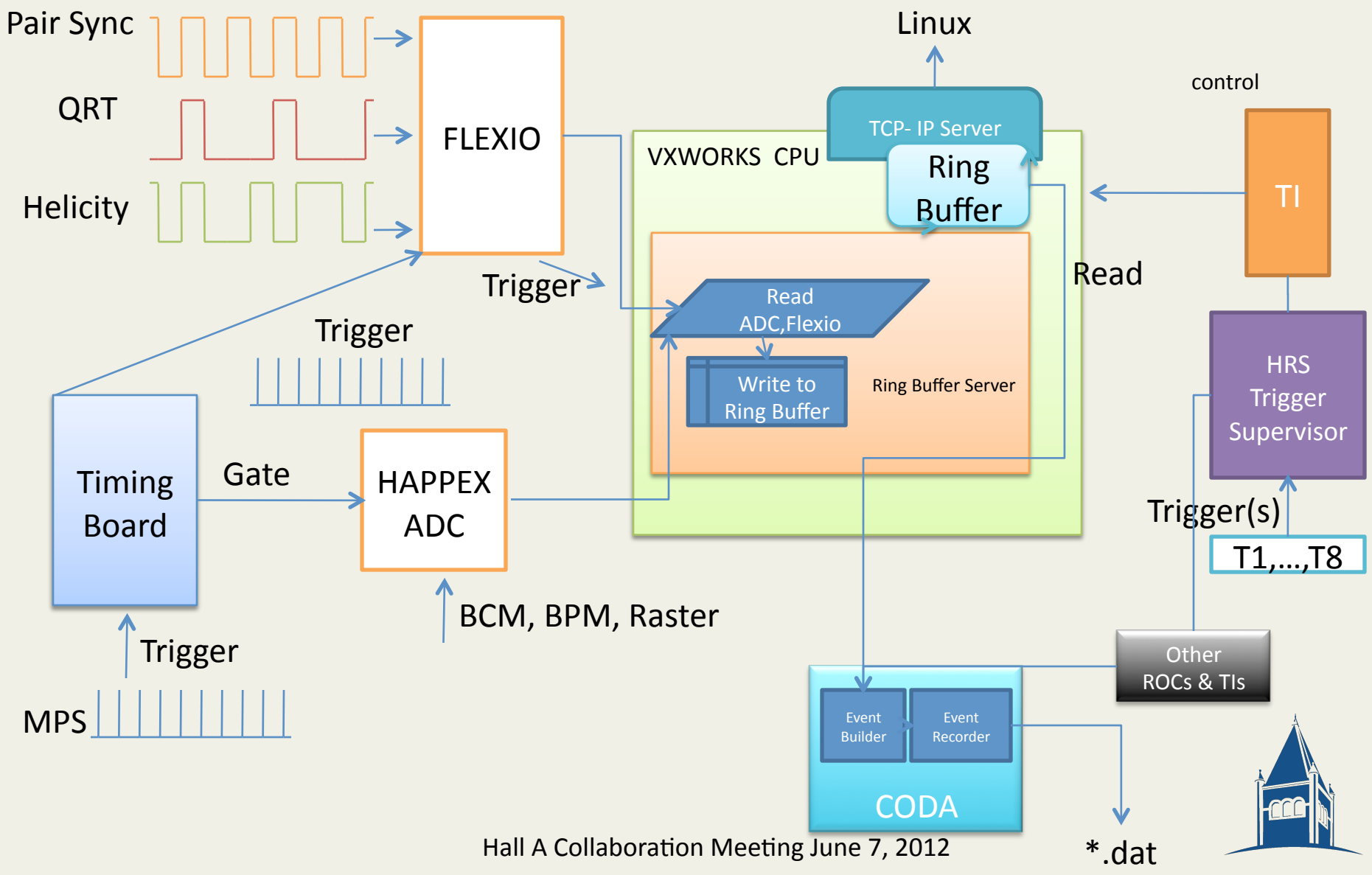
HAPPEX DAQ


Pair Sync
QRT
Helicity
FLEXIO
Trigger
Timing Board
Gate
HAPPEX ADC
BCM, BPM, Raster
Trigger
MPS
TCP- IP Server
VXWORKS CPU
Ring Buffer
Ring Buffer Server

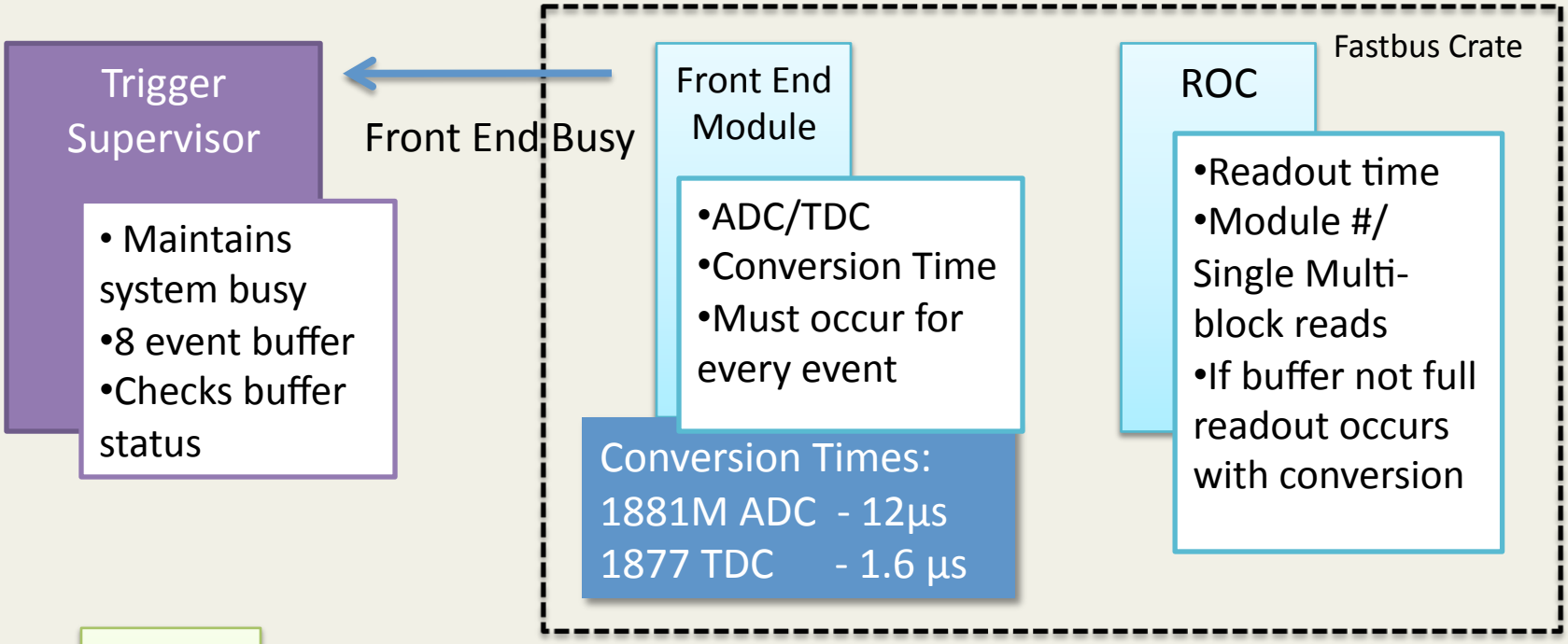
HAPPEX DAQ


Pair Sync
QRT
Helicity
FLEXIO
Trigger
Trigger
VXWORKS CPU
TCP- IP Server
Ring Buffer
Read ADC,Flexio
Write to Ring Buffer
Ring Buffer Server
Timing Board
Gate
HAPPEX ADC
BCM, BPM, Raster
Trigger
MPS

HAPPEX DAQ


Pair Sync
QRT
Helicity
FLEXIO
Trigger
Trigger
Linux
control
TCP- IP Server
VXWORKS CPU
Ring Buffer
TI
Read
Read ADC,Flexio
Write to Ring Buffer
Ring Buffer Server
HRS Trigger Supervisor
Timing Board
Gate
HAPPEX ADC
Trigger(s)
T1,…,T8
BCM, BPM, Raster
Trigger
MPS
Other ROCs & TIs
Event Builder
Event Recorder
CODA
*.dat

DAQ Deadtime



- Buffering separates front end time from readout time
- Scaler readout is tied to "sync events"
  - Sync events are unbuffered and check sync status of crates

Improving Deadtime

THIRD FASTBUS CRATE

- Third Fastbus crate added to each arm
  - Redistribution of modules lowers readout time
- Slowest crate dominates
  - ADCs add most to readout
- Fastbus transfer rate 20Mb/s

	Readout Time	Module Distribution
Roc 3	50.4 μs	8 TDCs (block read), 1 ADC
Roc 4	52.0 μs	8 TDCs (block read), 1 ADC
Roc 5	90.4 μs	2TDC, 4 ADC (3 are in block read)

ROC Busy Times – Measured with cosmics

Improving Deadtime

SFI SEQUENCER

- Implemented on software level
- Preprogram into SFI RAM Fastbus calls
  - Up to 40% improvement in execution time
- CRL code exists but only briefly tested
- Was not implemented for g2p

Thanks to David Abbott for his help!

Improving Deadtime

INTEL/LINUX CPU

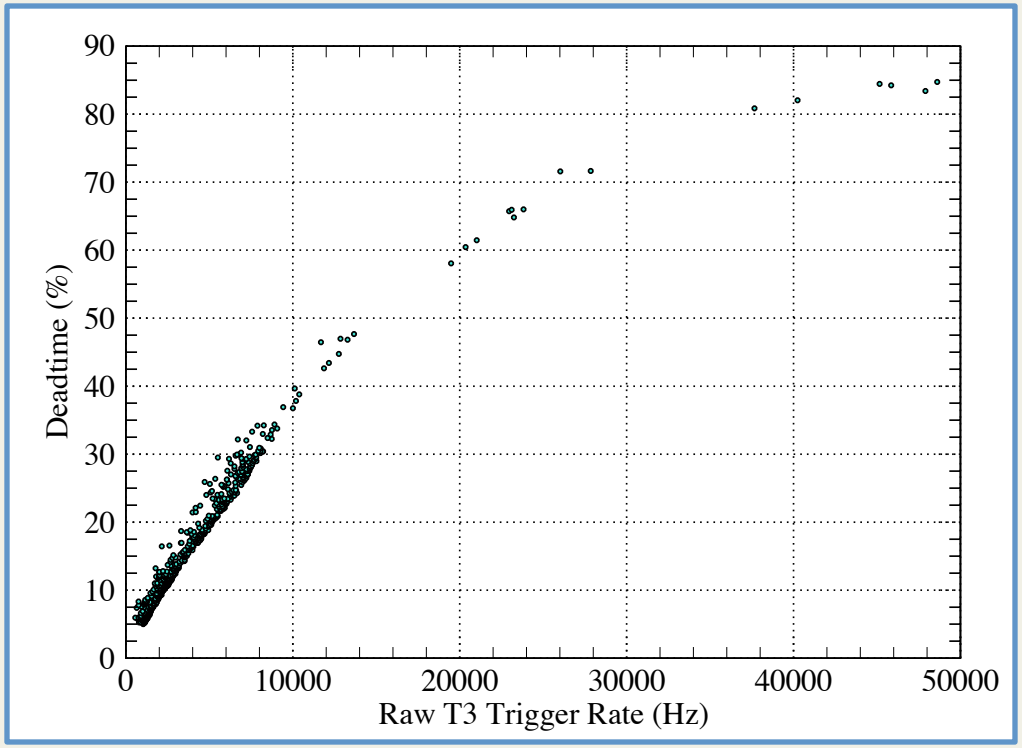
- Intel CPU successfully integrated into DAQ
  - Libraries now exist for 1877 TDC and 1881M ADC
- Did not see definite improvement in readout
  - Was not used in g2p
- SFI Sequencer not yet implemented for Intel

DAQ Performance

LHRS RESULTS

Production running **6.5 kHz** with ~**25% deadtime** with PS3 = 1!

Production Running



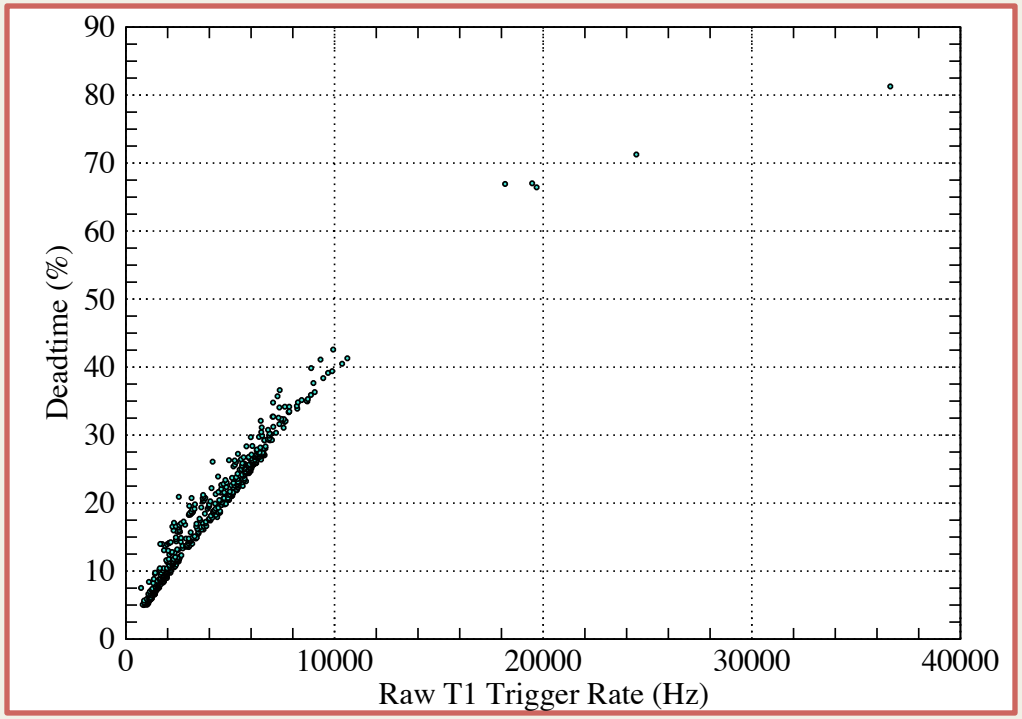
T3 (kHz)	PS3	DT (%)
6.5	1	25
15	2	20
22	3	20
30	4	20

DAQ Performance

RHRS RESULTS

Production running **6.1 kHz** with ~**25% deadtime** with PS1 = 1!

Production Running



T1 (kHz)	PS1	DT (%)
6.1	1	25
15	2	25
22	3	20
30	4	21

CONCLUSION

- Successfully integrated Happex DAQ into HRS DAQ
- Additional (third) Fastbus crate improved DAQ DT
  - Ran at 6.1 kHz (R) and 6.5 kHz (L) with 25% DT
  - Even higher if you prescale
- In the future…
  - Fully integrate SFI Sequencer
  - Replace VXWorks CPUs with Intel CPUs

THANKS!

- I would like to thank the following people who helped contribute to the DAQ success!
  - Bob Michaels
  - Alexandre Camsonne
  - Jack Segal
  - Vince Sulkosky
  - Melissa Cummings
  - Pengjia Zhu

ADDITIONAL SLIDES

DAQ Performance

DEADTIME MODEL

If the expected number of occurrences in a given interval is lambda, then the probability that there are exactly k occurrences (k = 0,1,2…) is

$$f(k;\lambda) = \frac{\lambda^k e^{-\lambda}}{k!}$$

- Can break down deadtime components into two infinite sums

$$D_c = \sum_{n=1}^{\infty} \frac{\mu_c^n e^{-\mu_c}}{n!}$$

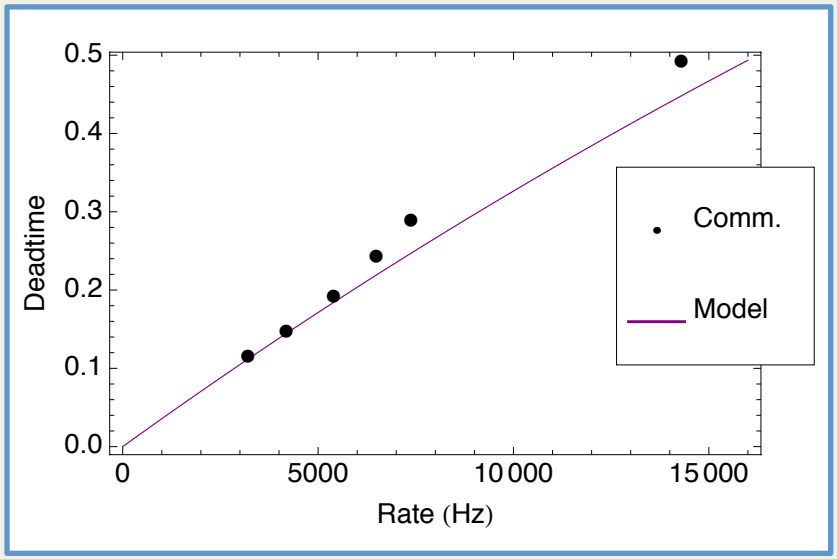
$$D_R = \sum_{n=1}^{\infty} \frac{\mu_R^{(n+b)} e^{-\mu_R}}{(n+b)!}$$

- b is the buffer factor, R is rate, $\mu_C = RT_C$, $\mu_R = R(T_R - T_C)$, T_C is conversion time, and T_R is the readout time

DAQ Performance

LHRS RESULTS!

- December commissioning data compares favorably to model

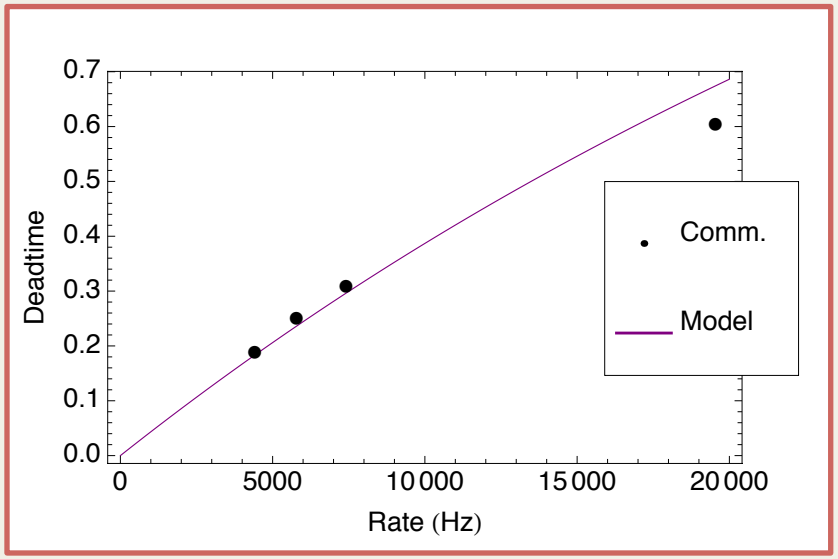


December Commissioning

Crate	T_c (µs)	T_R (µs)
Happex/TS		36
Fastbus	12	90

DAQ Performance

RHRS RESULTS!



December Commissioning

Crate	T_c (µs)	T_R (µs)
Happex/TS		44
Fastbus	12	100